Chapter 3 Simulation Model

3.1 Simulation model

In simulations, seven APTs are located as a linear network topology with the two APTs at both ends adjacent to each other. ATs in one of APTs are either distributed uniformly or proportional to the distance from APT, depending on the issue to be studied. The radius R of each APT is set to R= 500 meters. The maximum APT transmission power is 10 Watts, the default HIGH level power. The system bandwidth is W= 1.2288 MHz. Packet data transmission in a TDM fashion is determined every 1.67 msec, i.e., a time slot is 1.67 msec. Besides, we consider proportional fairness (**PF**) scheme as the packet data service scheduling strategy. In PF scheme, the parameter of window size is high at 1000 slots, long enough for an AT channel condition to improve, which hence improves system throughput [1]. The average data service size for one AT is 10 Kbytes.

The path loss model in chapter 2 is used where the path loss exponent α is typically between 2 to 5 [16]. Background noise is –170dBm as in [12]. Let the distance between an AT_i and its serving APT_j be $D_{i,j}$; Then the distances between the AT_i and other APTs are modeled (as in [15]) as follows:

$$\begin{cases} D_{i,k} = 2cR - D_{i,j} & \text{if } APT_k \text{ is on the right hand side of } APT_j \\ D_{i,k} = 2cR + D_{i,j} & \text{, otherwise} \end{cases} \quad (3\text{-}1)$$

where $k \neq j$ and constant c is the number of APT between APT_k and APT_j, including APT_j.

APT power has two levels, fixed maximum power (i.e., high power level) and reduced power (i.e., low power level). Different power pattern of seven APTs results in different SINR value for ATs. Table 3-1 below gives the target SINR for each data rate defined in HDR systems for equation (2-4) in chapter 2, we can calculate the corresponding E_b/N_o values which are also listed in Table 3-1. In simulations for discrete feasible data rate, we choose the rate set of 2457.6, 1228.8, 614.4, 307.2, 153.6, 76.8, and 38.4 Kbps.

Table 3-1 SINR for 1 percent packet error rate

Data Rate (Kbps)	SINR (dB)	E_b/N_o (dB)
2457.6	**9.5**	**6.49**
1843.2	7.2	5.44
1228.8	**3.0**	**3.00**
921.6	1.3	2.55
614.4	**-1.0**	**2.01**
307.2	**-4.0**	**2.02**
204.8	-5.7	2.08
153.6	**-6.5**	**2.53**
102.6	-8.5	2.28
76.8	**-9.5**	**2.54**
38.4	**-12.5**	**2.55**

In [6], the APT identity is generated randomly. For higher performance, we change the APT identity-given strategy which alternates even number and odd number in linear network topology. Besides, they showed that cell throughput for reduced power factor θ = 0.25 is higher than that for = 0.5, 0.75, and 1. Therefore, we still use the same reduced power ratio =0.25. The parameters of traffic and system models used in simulations are summarized in Table 3-2.

Table 3-2 Traffic Model and Simulation Parameters

Parameter	Value
Bandwidth (W)	1.2288MHz
Data Rate (c_i)	{2457.6, 1228.8, 614.4, 307.2, 153.6, 76.8, 38.4}
Cell Radius (R)	500m
Num of APT (M)	7
Background Noise(η)	-170dBm
Slot Size	1.67ms
Max. APT transmission power (P)	10 W
Ratio of reduced power (θ)	1/4
Long term fading standard deviation (σ)	5dB
Path loss exponent (α)	{2,4}
Average data Size	10Kbyte
PF window size (ΔWS)	1000 slots
Range of cell boundary user	1/2 cell radius

The following parameters are used for evaluating proposed adaptive power control scheme with one threshold (AP), adaptive power control scheme with two hysteresis thresholds (APH), and simple power control scheme (SPCS) in [6].

- *CC_EffAvgRate,*, *CB_EffAvgRate* and *SYS_EffAvgRate* : The effective average rate is defined to be the mean data rate over scheduled time slots for service. We will present the effective average rates in the cell-central zone, the cell-boundary zone, and the cell system, respectively. The cell-central and cell-boundary zones are divided at distance R/2 from APT.

$$EffAvgRate = \frac{\sum_{j=1}^{K_{actual\_trans.\_slots}(t)} packe\_size\_served_{AP_j}}{K_{actual\_trans.\_slots}(t)} \quad (3\text{-}2)$$

- *CC_AvgWTime*, *CB_AvgWTime* and *SYS_AvgWTime* : These are average waiting time of a user in the Cell-central zone, the cell-

boundary zone, and the cell system, respectively. The waiting time is calculated from the time when a service request arrives to the time when its service completes. The average waiting time is computed by

$$AvgWTime = \frac{\sum_{j=1}^{N_{dep\_user}(t)} WTime_{AP_j}}{N_{dep\_user}(t)} \quad (3\text{-}3)$$

where, N_{dep_user} means the number of departure user.

- *AvgPeriod*：The average period of the two-level power control.
- *L_AvgSlot*：The average number of slots in low power level once APT power level is tuned down. In other words, it is the mean lifetime time in low power level.
- *H_AvgSlot*：The average number of slots in high power level once APT power level is set to HIGH.
- *CB_L_SerProb*：The probability of a cell boundary user served in low APT power level.
- *CC_L_SerProb*：The probability of a cell central user served in low APT power level.

3.2 Pseudo Code for power control schemes

Several power control schemes have been introduced in the thesis. They are alternately described in the following pseudo codes. First, we define some variables in order to clarify notations used in the following algorithms:

ID(APT_i)：identity of APT_i for SPCS in [6].

CURRENT_SLOT：The number of slot at the moment

LOCK(APT_i)：If the power of APT_i had been setup and cannot be changed until next slot, the LOCK(APT_i) is true (**T**). Otherwise, the LOCK(APT_i) is false (**F**).

LOAD(APT_i), L_LOAD(APT_i), R_LOAD(APT_i)：These are defined that the cell loading of APT_i, the left-hand loading of APT_i, and the right-hand loading of APT_i.

POWER(APT_i) ：The power of APT_i has two levels, High (**H**) level and Low (**L**) level, respectively.

3.2.1 Algorithm and flow chart for SPCS

```
For i = 0 to 6
{
        If (CURRENT_SLOT is even )
        {
                If (ID(APTi)  is even )
                        POWER(APTi)=H;
                Else
                        POWER(APTi)=L;
        }
        Else
        {
                If (ID(APTi)  is odd )
                        POWER(APTi)=H;
                 Else
                        POWER(APTi)=L;
        }
} Next APTi
```

3.2.2 Algorithm and flow chart for FPCS

Algorithm：

For i =0 to 6

LOCK(APT_i) = F

Next i

While(LOCK for ANY APT_i is False)

{

Choose APT_i with minimum $\frac{LOAD(APT_i)}{R\_LOAD(APT_{i-1}) + L\_LOAD(APT_{i+1})}$

and the LOCK= F

If ($\frac{LOAD(APT_i)}{R\_LOAD(APT_{i-1}) + L\_LOAD(APT_{i+1})} \le \rho$)

{

$POWER(APT_{i-1}, APT_i, APT_{i+1}) = (H, L, H)$

$LOCK(APT_{i-1}, APT_i, APT_{i+1}) = (T, T, T)$

}

Else

{

$POWER(APT_i) = H$

$LOCK(APT_i) = T$

}

}

3.2.3 Algorithm and flow chart for APCS

Algorithm：

For each APT_i with $POWER(APT_i) = L$

If $\left(\frac{LOAD(APT_i)}{R\_LOAD(APT_{i-1}) + L\_LOAD(APT_{i+1})} > \varphi \times \rho \right)$

{

$POWER(APT_i) = H$

$LOCK(APT_i) = F$

If $(POWER(APT_{i-2}) \neq L)$

$LOCK(APT_{i-1}) = F$

If $(POWER(APT_{i+2}) \neq L)$

$LOCK(APT_{i+1}) = F$

}

Next APT

For each APT_i with minimum $\frac{LOAD(APT_i)}{R\_LOAD(APT_{i-1}) + L\_LOAD(APT_{i+1})}$ and

the LOCK=F

If $\left(\frac{LOAD(APT_i)}{R\_LOAD(APT_{i-1}) + L\_LOAD(APT_{i+1})} \leq \rho \right)$

{

$POWER(APT_{i-1}, APT_i, APT_{i+1}) = (H, L, H)$

$LOCK(APT_{i-1}, APT_i, APT_{i+1}) = (T, T, T)$

}